CLAIMS

1. Method for processing a low ohmic contact structure to a buried conductive layer in or below a device layer forming part of a semiconductor component, said method comprising providing a highly doped region within said device layer reaching said buried conductive layer

characterized in that

said providing said highly doped region is followed by etching a trench through said highly doped region to a final depth which extends at least to the semiconductor substrate underneath said buried conductive layer.

2. Method according to claim 1

characterised in that

said highly doped region is provided by means of a high-temperature doping step through an insulator masking layer,

whereby said insulator masking layer is also used for defining said trench region.

3. Method according to claim 2

characterised in that

said insulator masking layer includes an oxide layer as top layer.

4. Method according to claim 2

characterised in that

said high-temperature doping step is performed through a polysilicon layer which is deposited on top of said insulator masking layer.

5. Method according to claim 1

characterised in that

said providing said highly doped region is preceded by pre-etching said trench until a predetermined depth which is less deep than said final depth.

6. Method according to claim 4

characterised in that

said providing said highly doped region is preceded by pre-etching said trench until a predetermined depth which is less deep than said final depth.

7. Method according to claim 5

characterised in that

said predetermined depth is at minimum the depth of the upper edge of said buried layer minus the vertical outdiffusion depth of said highly doped region.

8. Method according to claim 6

characterised in that

said pre-etching of said trench is followed by the deposition of said polysilicon layer, whereby said highly doped region is provided through diffusion of a dopant through said polysilicon layer into said device region.

9. Method according to claim 1

characterised in that

said final depth of said trench is related to the maximum breakdown voltage between two buried layer regions separated by said trench.

10. Method according to claim 9

characterised in that

said etching of said trench until said final depth is followed by a *step of providing a stopper implant region beneath said trench*

whereby said maximum breakdown voltage is further determined by said stopper implant region.

11. Semiconductor structure including a trench in a device layer on top of a buried layer, said trench extending at least through said buried layer to a semiconductor substrate beneath said buried layer, said trench being surrounded by a doped region which vertically extends at least to the upper edge of said buried layer and which has a doping concentration which is higher and of opposite type than the doping concentration of said device layer.

12. Semiconductor structure according to claim 11

characterised in that

said semiconductor structure further includes a highly doped stopper implant region beneath said trench in said semiconductor substrate.